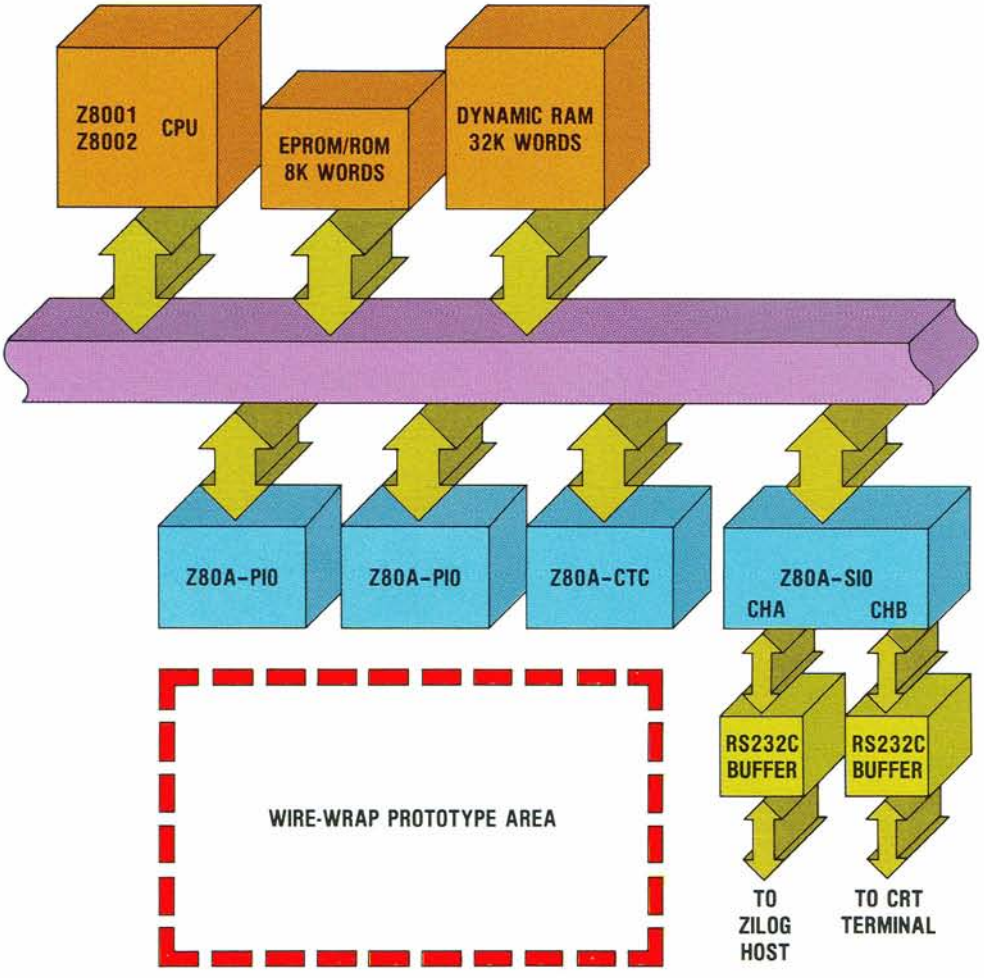
Z8000™ Development Module

Product Brief August 1979



Z8000 Development Module Block Diagram

Features:

- **Z8000 Microprocessor**
- **2K words EPROM (expandable to 8K)**
- **16K words Random Access Memory (expandable to 32K)**
- **Dual serial interfaces (110–19.2K Baud)**
- **32 programmable I/O lines with handshake controls**
- **Four programmable 8-bit counter/timers**
- **Wire wrap area (18 sq. inches)**
- **Jumper-selectable CPU clock rates**

Description:

The Z8000 Development Module is a complete, single board Z8000 microcomputer system specifically designed to assist the user in evaluating and developing hardware and software for Z8000-based products. It contains the Z8002 microprocessor, 16K words of dynamic RAM, 2K word monitor PROM, dual serial interfaces, four counter/timers and 32 programmable parallel I/O lines. The memory resources of the board may be easily expanded with the addition of 16K RAM and 2K EPROM components. A wire wrap area also allows for addition of custom interfaces or special applications circuits.

The Z8000 Development Module is a high-performance prototype system with designed-in flexibility to accommodate a wide range of user applications. A variety of jumper areas and switches permit:

- Selection of 2.5 or 3.9 MHz clock rates
- Use of 2708, 2716 or 2732 EPROM's
- Use of 4K or 16K Random Access Memories
- Serial interface to modem, terminal or teletype
- I/O port addressing
- Baud rate selection (110–19.2K Baud)

General:

The Z8000 Development Module communicates with the outside world using the two RS232C serial interfaces. For standalone operation a single jumper-selectable interface for RS232C or current loop is used to communicate with a console device. The other serial interface may be connected to a Zilog Microcomputer or Development System to allow downloading and uploading of program information, using a utility program in the host computer system. The Development Module is easily interfaced to the Zilog host with a cable connection; no additional hardware is required.

Software Features:

The monitor program, contained in 4,096 bytes of EPROM, provides the necessary debugging commands, input/output control and host interface for the Z8000 Development Module. It consists of a terminal handler, command interpreter, debugger and upload/download handler.

- Terminal Handler — provides interface to console device, either RS232C or current loop, to facilitate output to a display or printing mechanism and input from an alphanumeric keyboard.
- Debugger — provides a basic set of debug commands to allow the user to start and stop program execution easily, display and alter CPU register, flags or memory, and trap instruction sequences.

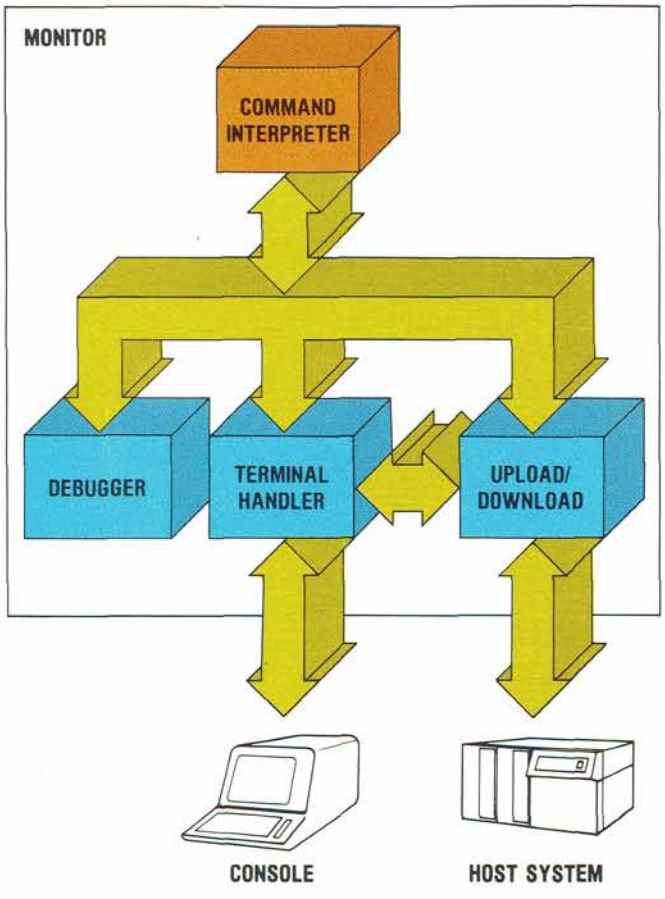


Fig. 1. Monitor Block Diagram

- Command Interpreter — scans console inputs, insures command validity and passes requests to other software modules in the 4K monitor.
- Upload/Download Handler — provides an interface between the serial connection and the host computer, the command interpreter and the memory resources of the Z8000 Development Module. It formats and interprets asynchronous data streams to and from the host and provides error checking and recovery for the serial interface.

Upload/Download Feature:

The upload/download feature allows data to be transferred from or to the Zilog host computer system. This feature requires that the Z8000 Development Module be serially connected to the Zilog host and console device. In this configuration the Z8000 Development Module serves as a message switcher and sits on the communications link between the console for the Zilog host and the console itself.

The execution of a LOAD or SEND command from the console invokes a data transfer sequence to or from the host. After successful transfer, control is returned to the console. Checksum errors are reported on the console and the transfer is aborted when the user depresses the escape key.

The format for transferred data blocks is illustrated in the figure below. This format is also used by the PUNCH and TAPE commands for paper tape input or output via the console device.

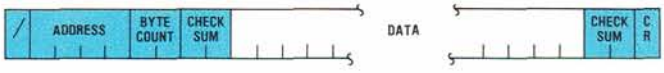
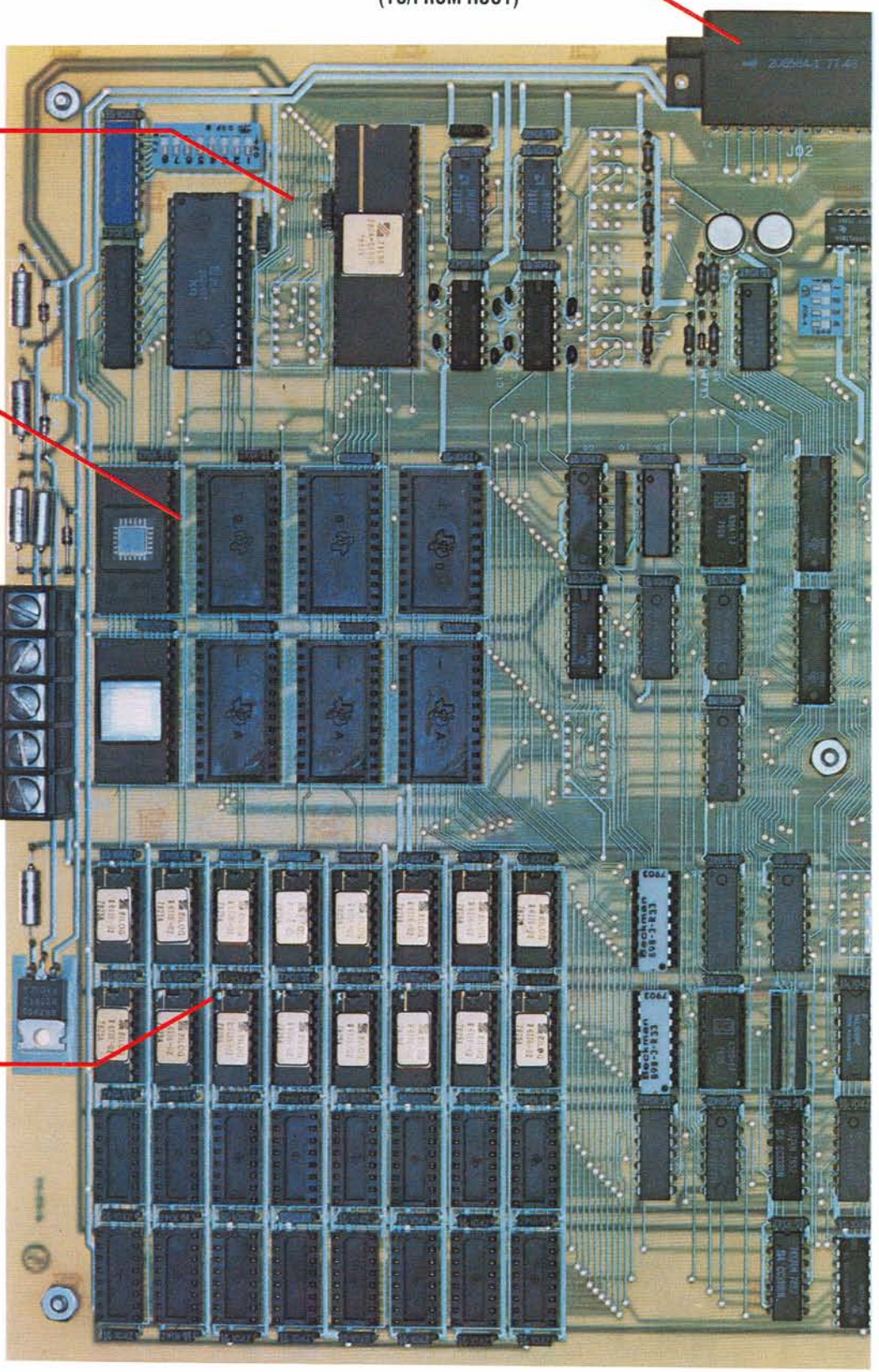
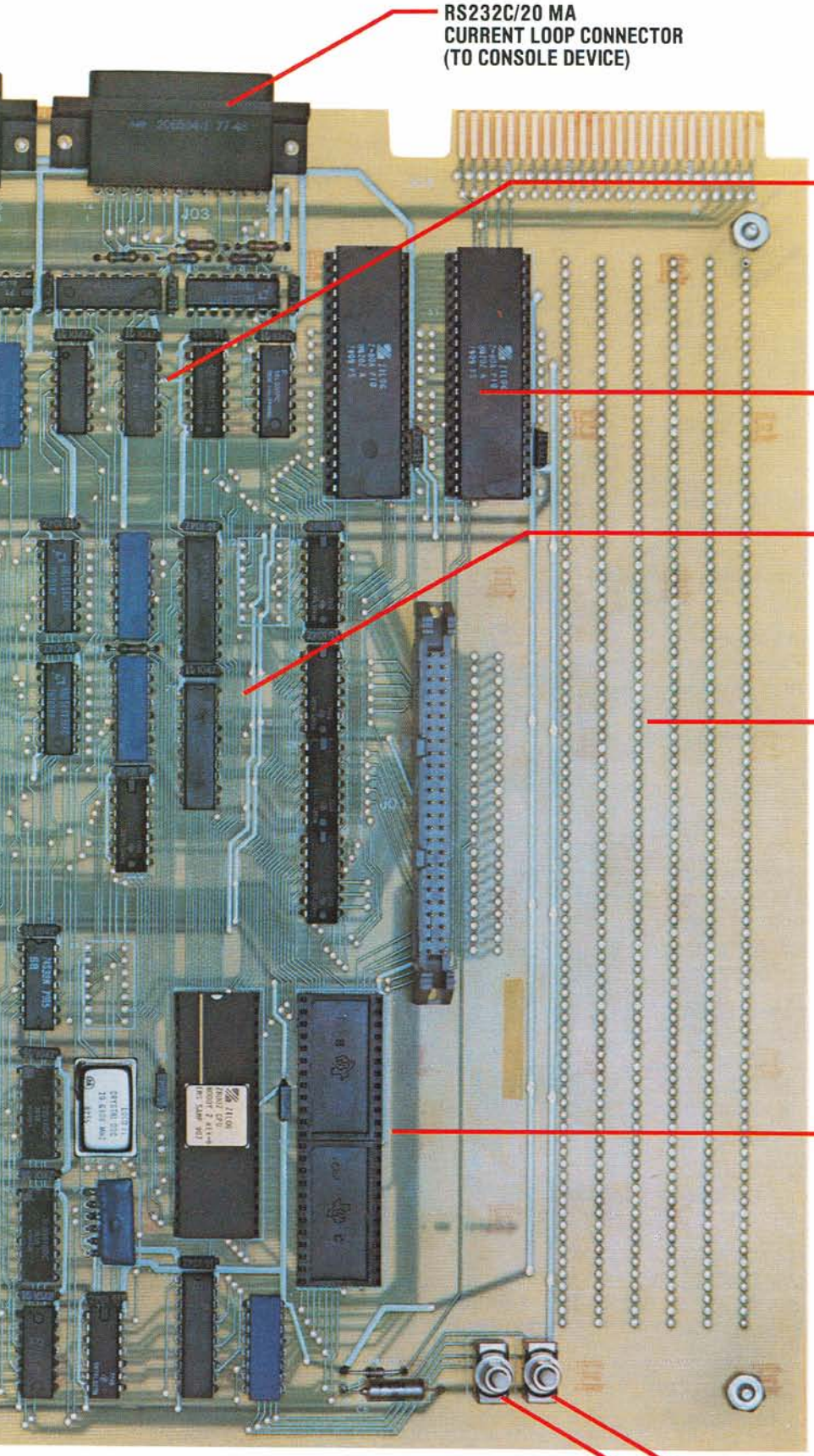


Fig. 2. Serial Data Format

Z8000 Development Module





RS232C/20 MA
CURRENT LOOP CONNECTOR
(TO CONSOLE DEVICE)

I/O INTERFACE LOGIC

- SELECTABLE ADDRESS RANGES
- INTERFACES Z80A PERIPHERALS TO Z8000 CPU BUS

PARALLEL I/O

- 32 PROGRAMMABLE I/O LINES
- HANDSHAKE CAPABILITY

CPU BUS INTERFACE

- BUFFERED Z8000 SIGNALS
- AVAILABLE USING J01
- AVAILABLE TO WIRE WRAP AREA

WIRE WRAP AREA

- APPROX. 18 SQ. INCHES
- USER APPLICATIONS DEVELOPMENT

Z8000 MICROPROCESSOR

- Z8001 AND Z8002 SUPPORTED
- JUMPER SELECTABLE CLOCK RATE

RESET SWITCH

NON-MASKABLE INTERRUPT SWITCH

Command and Summary:

The following notation is used in the command description.

< >	Enclose descriptive names for the quantities to be entered, and are not actually entered as part of the command.
[ ]	Denote optional entries in the command syntax.
|	Denotes "OR", eg. W|B denotes that either W or B may be used but not simultaneously.
BREAK <address> [<n>]	Sets and clears a breakpoint at a given memory address. The option <n> allows specification of the number of occurrences, where n is from 1 to 128. The default is one.
COMPARE <address 1> <address 2> <n>	Compares two blocks of memory data beginning with the addresses specified for <n> bytes, where n is from 1 to 128. Errors are reported on the console device.
DISPLAY <address> <n> [L|W|B]	Displays and modifies memory for <n> number of words or bytes. The optional entry allows data to be handled as bytes, words or long words. The default is words.
FILL <address 1> <address 2> <word>	Stores the <word> from memory address 1 to and including address 2.
GO	Begins program execution at the address contained in the current PC; execution is resumed where it was last interrupted. All registers are restored prior to execution.
IOPORT <address> [W|B]	Allows direct communications from the console to a selected I/O port. A word (W) or a byte (B) may be read from the selected port and a word or byte may be sent to the selected port; default is byte.
JUMP <address>	Unconditional branch to the specified address. All registers are restored prior to execution.
MOVE <address 1> <address 2> <n>	Moves contents of a memory block from source address <address 1> to destination address <address 2> for <n> bytes.
NEXT [<n>]	Executes the next <n> machine instructions. <n> may be from 1 to 128. If n is omitted 1 is assumed.
PUNCH <address 1> <address 2>	Punches a copy of memory from address 1 to address 2 on paper tape on the console device. Automatically turns on punch and a null leader is created. Upload/Download section describes the tape format used.
QUIT	Places serial channels into transparent mode. The Z8000 Development Module must be connected to both the Zilog host and the console device, and the Development Module acts as a message switcher.
REGISTER [<register name>]	Allows examination and modification of Z8000 registers. 8-bit, 16-bit or 32-bit quantities may be selected by the appropriate register-naming conventions.
TAPE	Loads memory from paper tape via the console device. The Upload/Download section describes the tape format used.

Specifications:

CENTRAL PROCESSOR	CPU: Z8002 Clock Rate: 2.5 MHz or 3.9 MHz
MEMORY	ROM: 2K words 2716 (expandable to 8K words) RAM: 16K words 6116 (expandable to 32K words)
INPUT/OUTPUT	Parallel: 32 lines (two Z80A-PIO's) Serial: Dual RS232C or RS232C and Current Loop (Z80A-SIO) Note:The user has access to all bus signals which allow custom system expansion into the wire wrap area or off-board.
INTERRUPTS	Maskable Vectored (256) Maskable Non-Vectored Non-Maskable Segmentation Trap
PHYSICAL CHARACTERISTICS	Height: 1.75in. 4.5cm Width: 14.0in. 35.6cm Depth: 11.0in. 27.9cm Weight: approx. 30oz. 850gm
D.C. POWER REQUIREMENTS	+5V, 3A +12V, 1A −12V, 0.2A

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