NAKED MINI/ALPHA 16

The ALPHA/NAKED MINI concept

In creating ALPHA™ and NAKED MINI,™ we had some simple, yet very ambitious goals.

We wanted to offer a minicomputer that was — above all — easy to use. Even more, it had to be dependable and very low in cost. With no sacrifice in computer power.

By establishing these goals, we committed ourselves to the creation of a whole new kind of minicomputer.

Where "easy to use" means just that: easy to learn, easy to understand, easy to program, easy to interface, and easy to maintain.

Where dependability means day-in, day-out reliability even in tough field use.

Where computing power means fast "getting-the-job-done" time, not raw cycle time.

Where low cost means standard features usually found only as options in the expensive computers (and sometimes not even there). The first low-cost computer that's still a low-cost computer by the time you get it.

The NAKED MINI 16

Sometimes you need real computer performance even when your budget is tight.

That's why we designed the NAKED MINI 16. It's a parallel 16-bit general-purpose computer. With full computer performance at very low cost.

Not as a kit. Not as a collection of modules and pieces.

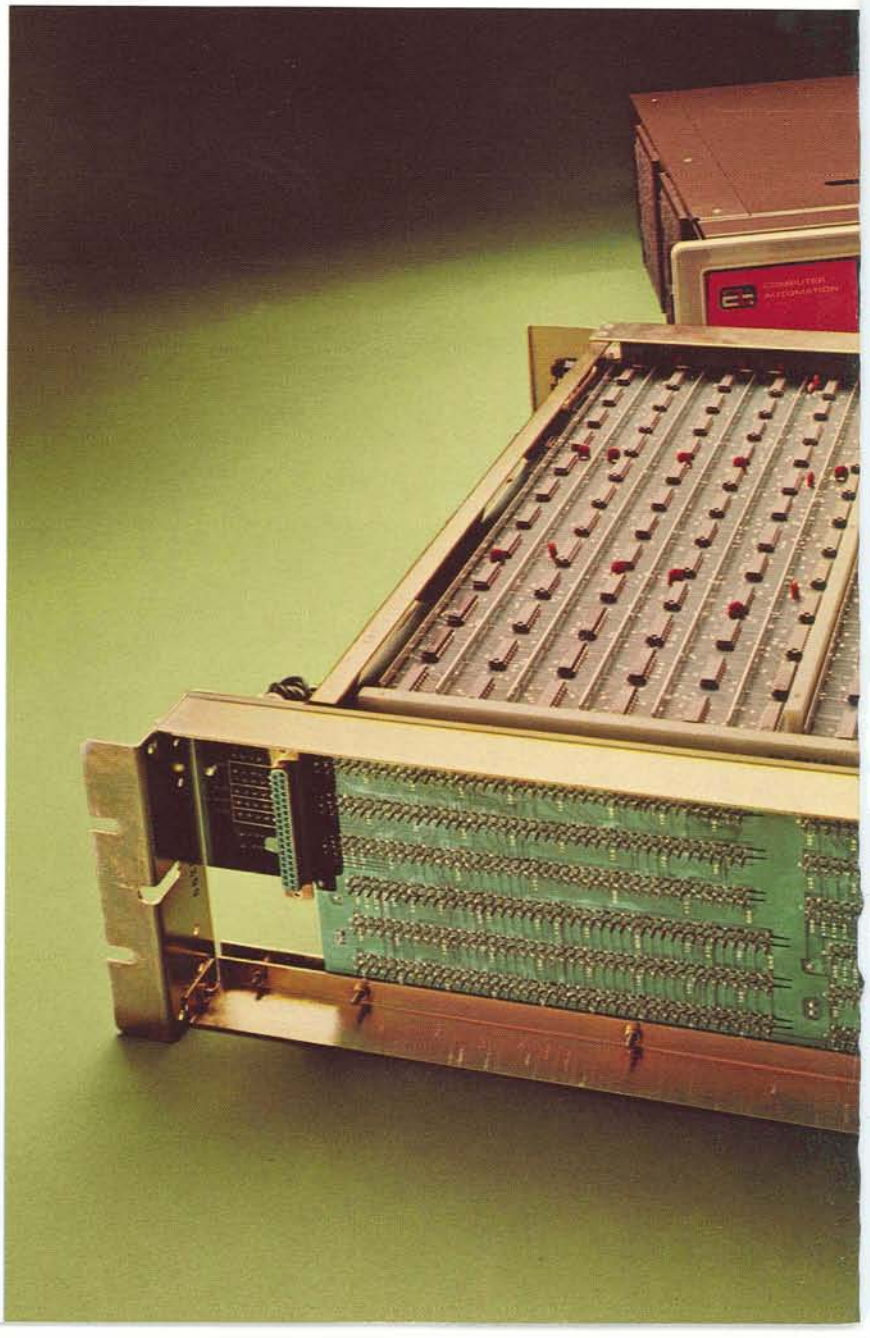
But as a complete, fully-operational computer that includes a core memory expandable to 32K words.

From the beginning, it was designed as a dependable building block. A component you could integrate easily into your own system.

With 1600-nanosecond cycle time and even greater performance than our widely accepted, earlier 16-bit minicomputers.

As standard, it comes without a control panel or power supply. You provide those as part of your own system, or we supply them as options.

The NAKED MINI is naked. But it's not stripped. And that's the important difference.



NAKED MINI™16 (foreground), a fully-implemented processor. Designed as a dependable component ready to bury into your system. All you have to add is a control panel and power supply. For OEM users, it means full computer capability at less than the cost of special-purpose hardwired circuitry.

ALPHA™16. For stand-alone applications, we take a NAKED MINI 16 and add a control panel and power supply. The result is ALPHA 16. Same great dependability and processing power. ALPHA 16 and NAKED MINI 16. The difference is only skin deep.

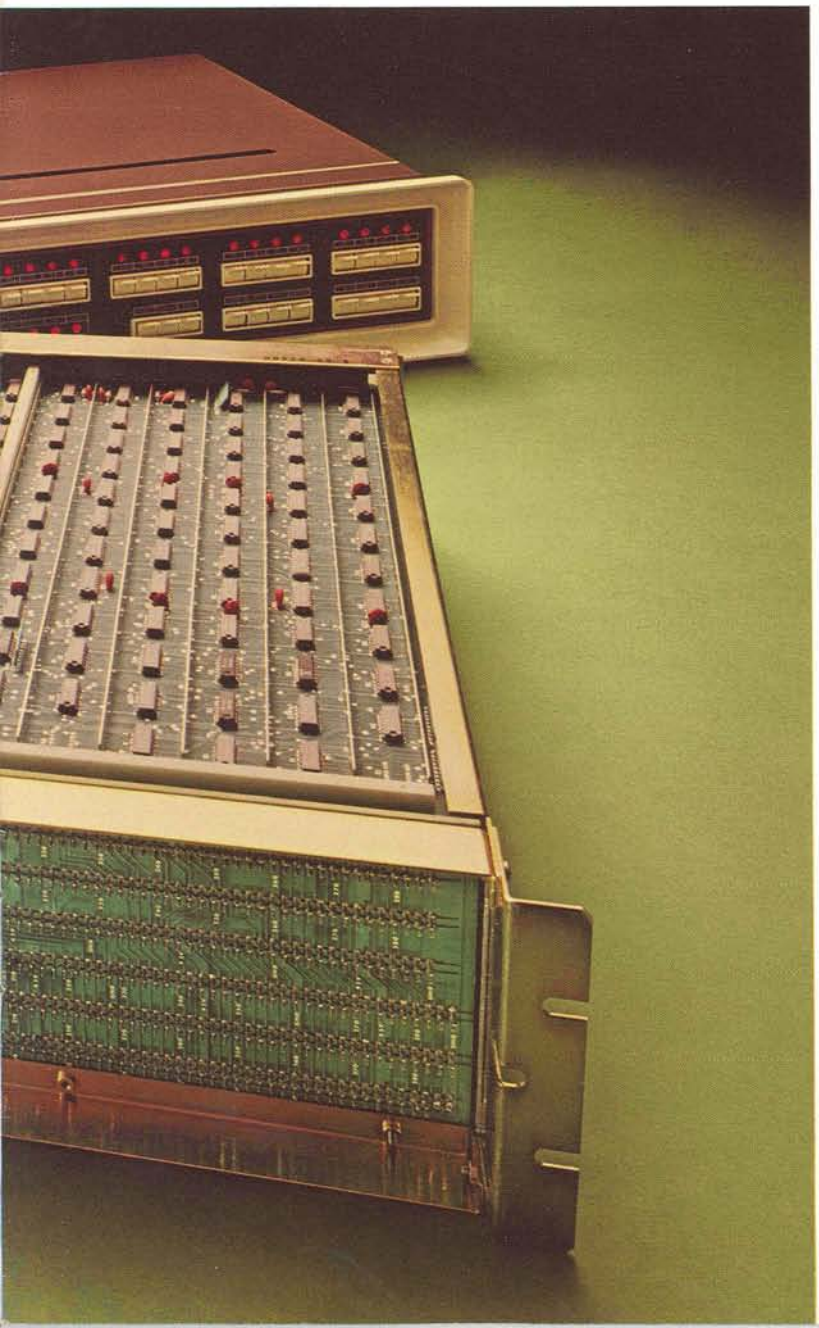
The ALPHA 16

For stand-alone applications, take a NAKED MINI. Add a control panel and a power supply. The result is ALPHA 16.

Same great dependability and computing power, all in a complete package.

With a wide variety of peripheral equipment. And special interfaces too, if you need them. Plus a comprehensive selection of advanced systems software.

ALPHA and NAKED MINI. The difference is only skin deep.



Features

Quality construction

Full *one-year* unconditional factory warranty.
High reliability — IC burn-in to MIL-STD-883
Light-Emitting Diode Display

Powerful instruction set for shorter programs

Hardware Multiply/Divide (standard)
Single word instruction format
Extensive byte capability
Immediate instructions
Memory Scan
3-way compare
Variable increment shifts
Full logical instructions: OR, XOR, AND, NOR
Conditional Jumps
Double register rotates, logical and arithmetic shifts
Register change instructions

Comprehensive OEM software

Four operating systems
BASIC
FORTRAN
Conversational and Batch Assemblers

Efficient hardware

Relative addressing — no paging
Multi-level indirect addressing
Vectored priority interrupts (up to 256)
Two general purpose registers including index
Five Input/Output Systems
- Direct Memory Access (DMA)
- Two Direct Memory Channels (up to 128)
- High Speed Block I/O to memory
- Programmed I/O to A or X
- Conditional I/O

Convenience features

Console Interrupt
Remotable Operator's Console with key lock
Modular, quick disconnect power supply
Five sense switches
Remote Autoload

Quality with economy

Quality counts. It's what keeps operating costs low and field problems few.

But true quality and reliability — the kind that keeps your systems going day in and day out — don't just happen. They have to be designed in, manufactured in, inspected in, burned in, and — above all — tested in. The strictest standards have to be applied and kept the hard way: step by step.

At Computer Automation, we don't cut corners with machine performance to save money. Instead, our high quality at low cost comes from advanced design and manufacturing techniques. It's harder that way . . . but it results in a better product at a lower price.

And this continuing insistence on quality and reliability is nothing new. It's been an integral part of every product we've designed.

In our earlier machines of this 16-bit family, the result was an unusually high level of reliability in actual field use.

Now, you can expect even better reliability from your ALPHAs and NAKED MINIs.

Design.

It all starts with a very conservative design philosophy. To give you just a few examples, we pay careful attention to minimizing system noise to prevent problems. Even in this design phase, we concentrate on making the computer easy to build and check out.

To make all major subsystems quickly and easily accessible for service, we keep mechanical package design simple. We use large printed circuit boards, to minimize interconnections. We plug them into a common connector panel, which also makes all external connections for peripheral devices. This *totally* eliminates the less reliable wire wrap connections required on most other minicomputers.

For even greater reliability in applications where they are needed, we provide important optional features not usually found in other minicomputers. These include memory parity checking and memory protect.

Component Test.

To make sure our components are right before we build them into anything, we put them through three tough tests, including MIL-STD-883. First a thermal shock test. Next, a long burn-in for 168 hours. Finally, a 100% functional and DC parameter check.

We catch most potential problems here, early in the process, before they cause trouble and extra expense.

Modules undergoing complete tests before system assembly.

Manufacturing.

Here's where careful design and manufacturing know-how pay off. For example, we control the quality of the soldering on our printed circuit boards more carefully because we use a protective solder mask. Not only does this result in better boards, but later on it helps protect against potential shorts in handling and trouble-shooting. This is of special importance in the field, when you're building our computers into your system and maintaining them.

Module Test.

We test our completed circuit boards in two ways.

First, we use our own computer-controlled automatic tester, called CAPABLE™. It checks the entire board thoroughly, pinpointing any errors for correction.

Next, boards which pass the first test are swapped into an otherwise completely checked-out computer, where we run exhaustive Quality Control diagnostic programs.

System Test.

Each computer, newly assembled from previously tested circuit boards, is given a complete overall system test.

First, we run full diagnostic programs to verify proper operation, including checking for maximum memory size and all input/output functions.

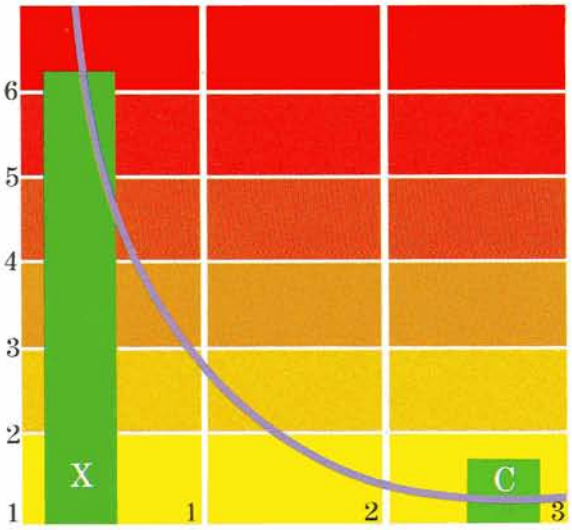
Next, a high temperature test in an oven. We cycle the temperature up to 50° C. and back down twice, continuously running Quality Control Diagnostics.

Finally, what we think is the longest burn-in period in the industry. We burn-in each computer for at least five full days, while we cycle power on and off at least 2,000 times. We run Quality Control Diagnostics during this entire period. If a single error occurs, we start that unit over.

When we finally give each computer its pre-shipment final inspection, we know it's right.

If a new computer is going to fail, chances are it would happen during the first three months of usage. That's why each NAKED MINI or ALPHA, with all the testing described above, goes out the door with the equivalent of three months' field operation under its belt.

We catch the failures here so you won't have to.



Most minicomputer manufacturers do little burn-in and ship at point "X". Computer Automation's burn-in is the longest in the industry. We ship at point "C" to save you problems.

Computers in burn-in undergoing pre-shipment inspection.

Powerful instructions for shorter, faster programs.

There's a big and very important difference between raw cycle time and "getting the job done" time. We believe computers should work smart, not hard. They should offer built-in features that assure faster execution.

With ALPHA/NAKED MINI, you get what many consider to be the most powerful instruction set on the market. With 152 basic instructions plus a superior logic structure, the ALPHA/NAKED MINI offers better memory efficiency than other 16-bit mini's.

This lets you write shorter programs with faster run times — and keeps memory costs to a minimum, since tasks run in less memory. And programs are easier to write, too.

In short, you get speed where it counts: on the job.

Memory Reference Instructions. In typical minicomputer applications, the computer usually spends a large percentage of its execution time successively doing one or a few operations on each of many pieces of data stored in tables in memory — rather than performing repeated calculations on just a few pieces of data which could be stored in registers. This usually means that memory is referenced frequently.

ALPHA/NAKED MINI optimizes its instruction set for these typical minicomputer applications, to get greater efficiency and ease of programming. It provides an extremely varied and powerful set of 26 memory reference instructions.

For example, in one step the ALPHA/NAKED MINI instruction ADD causes the contents of a specified memory location to be added to the contents of the A register.

By comparison, in register-oriented machines without this memory reference ADD instruction, a second register must first be loaded from the memory location and only then, as a second step, can a register-to-register addition be performed. The two-step process requires an extra instruction, an extra memory cycle, and an additional register to accomplish the same function. The same is true for other arithmetic, for compare, and for logical instructions.

Multiple Index Pointers. ALPHA/NAKED MINI provides indirect addressing. Coupled with the Increment Memory And Skip On Zero instruction, indirect addressing permits any number of memory locations to be used as index register pointers, quickly and simply.

High temperature testing to verify long-term reliability.

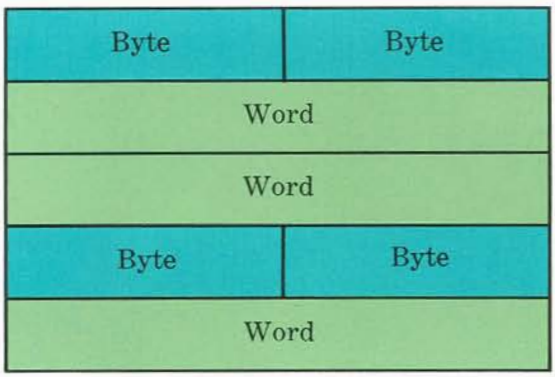
Memory Scan. Here's a good example of multi-function instructions which, in other computers, would require time and memory-consuming subroutines. Scan provides a rapid search of any portion of memory for any word or half word, with a speed equivalent to a machine with a cycle time three times faster. Any contiguous block of memory can be scanned (at a rate of 2000 nanoseconds per word) to see if it compares.

Three-Way Compare. This comparison instruction, occupying only a single memory location, gives the complete answer. It compares the contents of the selected memory location against the A register and jumps to one of three separate locations, depending on the results of the comparison — high, low, or equal.

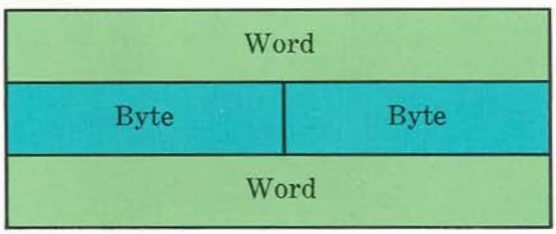
Word and Byte Addressing. We provide both word and byte addressing for most of the memory reference set. This means that you can deal directly with either bytes or full words, as the application requires, without the complications required in computers without byte addressing.

It is no longer necessary, as in most minicomputers, to use slow-running, memory-consuming byte pack/unpack subroutines.

On input/output, of course, byte addressing permits bytes to be packed/unpacked automatically by the hardware, or to be handled one byte per word, whichever is more convenient. An important feature since most peripherals are byte-oriented.



True word and byte addressing permit words and bytes to be intermixed in memory as desired.



Single Word Instruction Format. With the exception of a few multi-function I/O instructions, all ALPHA/NAKED MINI instructions require only one memory location. Compare this with many other minicomputers which require two or more memory locations for more than half of their instructions.

Full Shift Capability. ALPHA/NAKED MINI provides a full complement of 20 shift instructions which can be: single or multiple place; left or right; single or double register; and end off (logical), circular (rotate), or arithmetic. Compare this with the basic single place shift found in most minicomputers.

Fast, Efficient, Conditional Jumps. The 63 conditional jump instructions test conditions within the processor (overflow, sense switches, A and X registers) and perform conditional jumps depending upon the results. Each single instruction causes both the test and the jump, in only one cycle, saving both memory and time compared to other computers which need two words.

Exchange Memory. This instruction exchanges the contents of a memory location and the A register in a single instruction. Most minicomputers require three instructions to achieve the same result.

Multiply/Divide. Almost all minicomputers offer hardware multiply/divide instructions only as an extra cost option; slow and inefficient, memory-consuming programmed subroutines are the only alternative if the option is not purchased. We provide a more effective, lower-cost solution: the instruction set includes as standard the instructions Multiply Signed and Divide Signed, which provide the "heart" of fast, short Multiply and Divide routines.

Immediate Instructions. Unlike most minicomputers, and like modern large computers, ALPHA/NAKED MINI comes with a full complement of eight immediate instructions. The address portion of the instruction actually contains the 8-bit operand itself, rather than an address. This has two important advantages: only half as much time is needed, since the operand is in the instruction itself; and only half as much memory is needed, since both instruction and operand are contained in a single word.

Immediate instructions combine instruction and 8-bit operand in a single word.

Register Change. More than 30 register change instructions provide a wide variety of operations (zero, minus one, plus one, decrement, increment, negate, complement, transfer, NOR, AND, etc.) on the A and X registers.

Five input/output modes for maximum power.

Five different input/output systems, combined with the most complete set of I/O instructions (33) of any computer in its class, give ALPHA/NAKED MINI the most powerful and easy to use I/O structure in the industry.

For example, transfers can be made into the A or X registers or directly into memory, whichever is more convenient.

Both word and byte data can be handled directly, with byte data being packed automatically, if desired, without the need for time and space-consuming programmed routines.

Further, the large set of I/O instructions and systems coupled with a straightforward I/O interface philosophy makes ALPHA/NAKED MINI easy to interface and easily adaptable to a very broad range of applications.

Direct Memory Access (DMA). For very high speed transfer rates, the DMA handles data directly with the memory at rates up to 714,000 words/second or 1,428,000 bytes/second. Since this data transfer does not require the central processor, it can be performing other operations while interleaving with DMA on a cycle stealing basis.

Block Input/Output. For high speed transfer rates, Block I/O transfers blocks of any length at rates over 416,650 words or bytes/second. Data is exchanged directly between memory and the peripheral interface with the index register providing the word count.

Programmed Input/Output. For greater convenience in dealing with I/O where data must be examined immediately upon input or is the result of computation which must be output immediately, Programmed I/O provides data transfers directly with the A or X registers at speeds up to 119,000 words or bytes/second. Programmed I/O is especially useful in dealing with byte transfers, such as message handling or compiler operations.

Conditional Input/Output. Programmed I/O instructions can be combined with Sense-and-Skip instructions to allow testing prior to transfer in a single instruction. This takes only one memory word and only one instruction time. This is a faster method of programmed I/O and is convenient for fast response. For example, when dealing with magnetic tape, Sense For Ready and Input can be combined in the Read instruction.

Direct Memory Channels (DMC; 2 standard, up to 128 maximum). DMC transfers data without disturbing working registers at transfer rates up to 100,000 words or bytes/second. Any size block may be transferred into or out of memory at any address. Word Count and Current Address for each DMC are held in memory; each transfer automatically updates Count and Address until the count is complete. Multiple DMC's can operate concurrently. The DMC uses vectored priority interrupts in conjunction with the Automatic I/O instructions.

Final inspection of art work prior to printed circuit board manufacture.

Hardware priority interrupts

Hardware priority interrupts mean *automatic* handling of:

- recognition of an external event which requires immediate attention;
- identification of which event occurred among many possibilities; and,
- assignment of priority when several events occur simultaneously.

It also means really *fast response* to the event which caused the interrupt.

With ALPHA/NAKED MINI, it is no longer necessary to write the traditional complicated software routines to periodically store processor status, then to examine the external world to see whether an event has occurred, then to identify which of several possible events it is, then to determine whether this event has higher priority than another event which occurred previously, and only then — long after the event has actually occurred — to respond to that event.

Interrupts are recognized quickly, as soon as the current instruction is completed, usually within 1600-2000 nanoseconds. The necessary interrupt routines are simple, easy to write, take less memory space, and execute more quickly. Wasteful polling is completely eliminated.

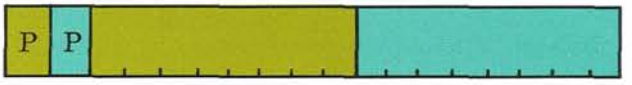
Because ALPHA/NAKED MINI has many multi-function instructions, it is frequently possible to perform the equivalent of an entire interrupt subroutine in a single instruction. In such cases, the interrupt can be recognized and responded to without jumping from the program currently being executed. This is possible because the Vectored Priority Interrupt System allows the execution of a single instruction in this way.

The Vectored Priority Interrupt System provides three interrupts as standard, with up to 256 optional. Each interrupt line is assigned a unique address which is supplied by the external source and can be assigned by the user.

Processor options

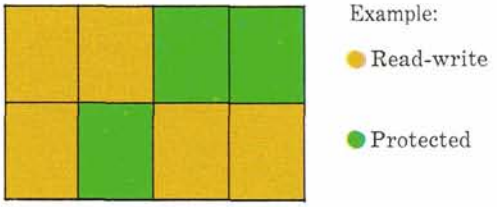
To increase the flexibility of ALPHA/NAKED MINI for various applications, we offer a number of processor options, including:

Memory Parity. Generates and checks parity on each memory transfer and provides an interrupt if an error is detected.



Since we offer both word and byte operations, we provide one bit of parity for *each byte* of memory when the Memory Parity option is implemented.

Memory Protect. Allows selected segments of core memory to be protected by preventing memory write operations in those segments.



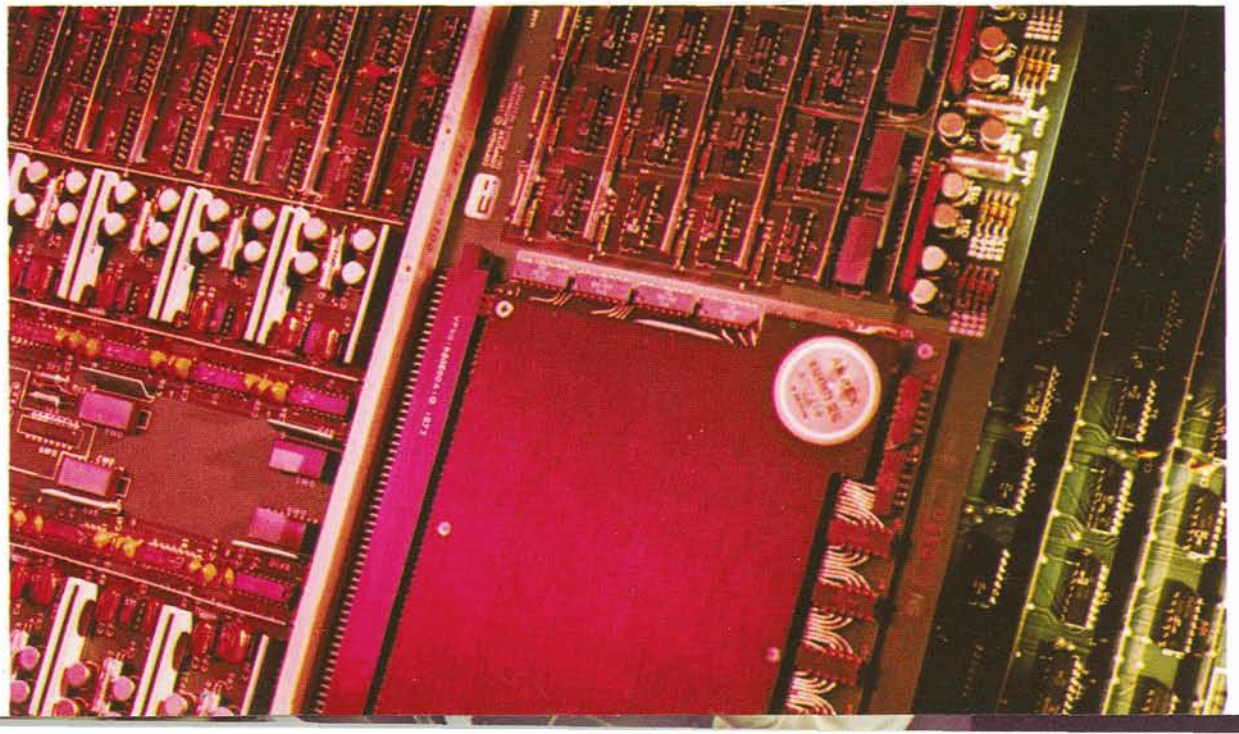
Autoload. Allows program loading to be initiated automatically by a front panel switch.

Power Fail Restart. Monitors secondary voltage to provide an orderly shutdown upon power failure and automatic restart when power is restored.

Real Time Clock. Provides interrupts at jumper selectable frequencies of 0.1K, 1K, or 10K Hz. External frequency source may be substituted.

Read Only Memories. 256 to 4096 16-bit words of read only memory and all necessary electronics mounted on a single module which plugs directly into one of the pre-wired chassis slots with no wiring modification. Interchangeable with core.

Memory boards have capacities of 4K or 8K words.



Peripheral equipment

The ALPHA/NAKED MINI product line includes a wide variety of standard peripheral equipment in most major functional types, such as teletypes, paper tape readers and punches, line printers, card readers, magnetic tape units, digital cassettes, magnetic drums, fixed head per track disks, and moving head disk units.

We offer the entire device, complete with interface, or just the interface alone.

Communications equipment

A good and growing selection of communications interface equipment is available, including data set controllers of various types, communications multiplexers, an autodialler controller, and a dual teletype/CRT/modem interface.

General purpose input/output interfaces.

We offer a number of general purpose input/output interfaces, already designed and in standard production. New interfaces are being added constantly. Some representative units:

16-Bit Input/Output Module. Provides a 16-bit input/output compatible with DTL/TTL, with control and sense lines.

Relay Output Module. Provides a set of 32 relay contacts which may be used to drive lamps, external relays, etc.

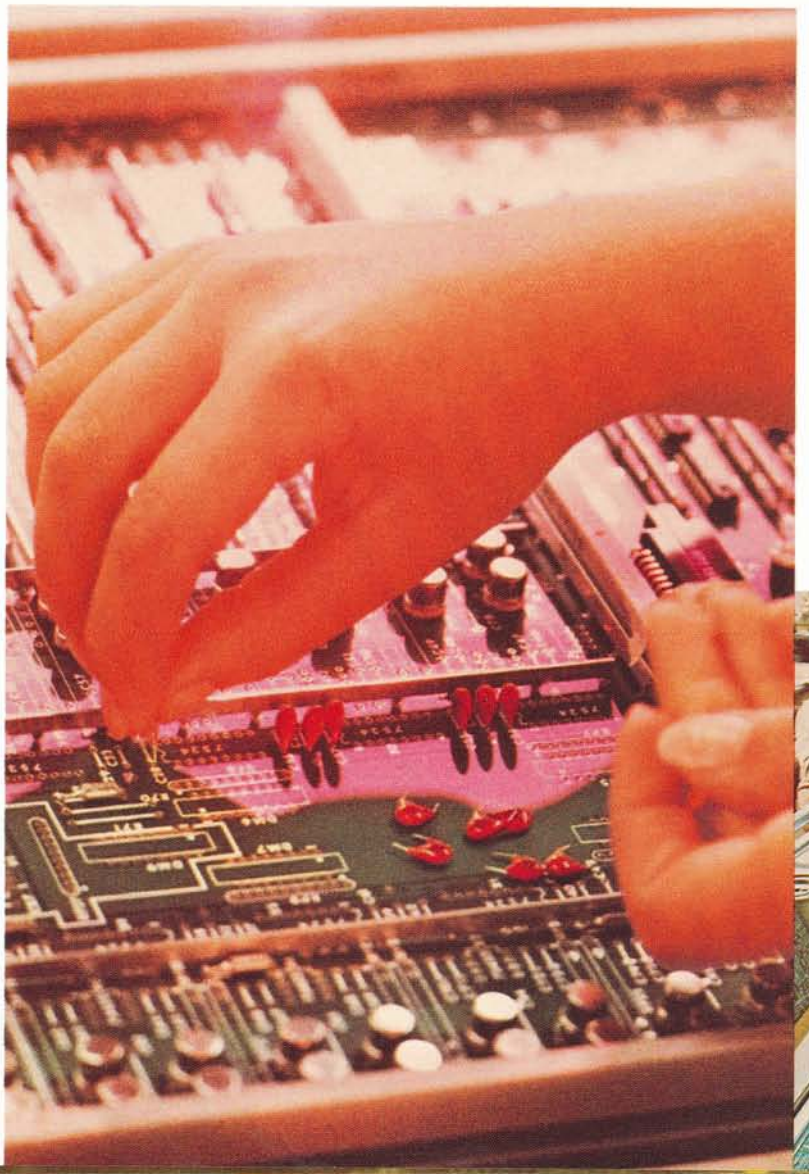
Relay Input Module. This unit presents 32 relay coils to the external environment. The contacts of these relays are presented to the processor's I/O bus.

64-Bit Output Module. Provides 64 DTL/TTL compatible outputs which may be used as a single output 64-bits wide or addressed and strobed in groups of 32, 16, or 8 bits.

64-Bit Input Module. Provides 64 DTL/TTL compatible inputs which may also be used in groups of 16 or 8 bits for multiple devices.

Priority Interrupt Module. Provides 16 inputs with individual antibounce circuits and change of state detectors. For use with momentary or toggle switches for operator initiated interrupts or as a general purpose priority interrupt module.

I/O Driver Module. Permits extending the processor I/O bus up to 25 feet from the processor. Also permits up to four computers to share the same I/O devices.



Pretested components being assembled and inspected.

Software

To support ALPHA/NAKED MINI, we offer a broad and constantly growing array of advanced systems software. It starts with compact, economical systems and programs which run in minimum hardware configurations. It goes to powerful systems — including higher level languages — designed to get maximum results from larger hardware configurations. Convenience and ease of use are emphasized. Wherever possible, software is modular in construction for greater flexibility.

Operating Systems

Real Time Executive (RTX). A good example of software specifically engineered to help get an OEM user and his product on the air fast. RTX is a powerful multitask executive program which helps the user quickly construct efficient real-time programs for his application. RTX does this by completely handling the usual real-time overhead functions, leaving the user free to concentrate on his application program.

Despite its small size (less than 650 words), RTX capability includes Task Control over all parts of the overall real-time program; Priority scheduling, response and assignment; Interrupt servicing, including fast interrupt response; and Task Communication among RTX tasks and user-developed handlers.

Using the Real-time Debug program under RTX, the user can actually examine his application program and make any changes necessary to correct or improve it, all while the real-time program is operating.

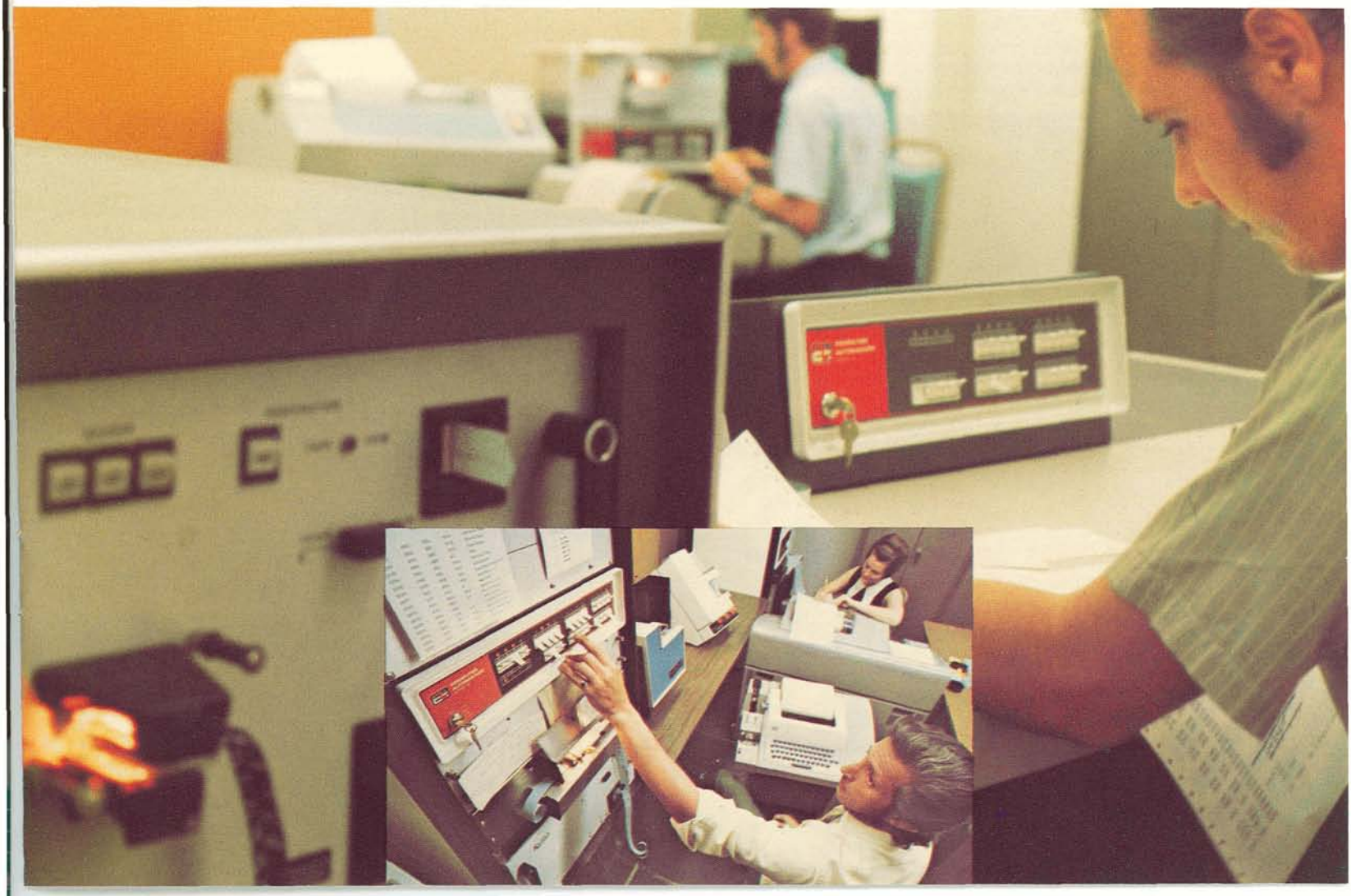
Finally, RTX is modular in construction, which means only those program modules actually used in a particular application need be stored in memory. This leaves even more room for the application program itself.

Disc Operating System (DOS). DOS provides a comprehensive capability for dealing with files of virtually any length, providing both random and sequential access. It is device-independent and handles all user input/output, including interrupt-driven service of all devices. It may be used with any Computer Automation disc or drum storage system of appropriate size.

Magnetic Tape Operating System (MTOS). Functionally equivalent to DOS, except it uses industry compatible open reel magnetic tape drives.

Cassette Operating System (COS). Functionally equivalent to DOS, except it uses a digital tape cassette instead of a disk.

Development of software systems in the programming laboratory.



Higher Level Language Compilers

Advanced BASIC. Implementation of the interactive BASIC language as it was developed at Dartmouth College. All Elementary and Advanced BASIC statements run in only 4K of memory with dynamic memory allocation. In addition, we have added extra features like recursive subroutines nested to any level, extended depth of expression in equations, and the capability to accept expressions, subscripts, and arguments as input data. Also included is a Calculator Mode, for immediate execution of statements.

Extended BASIC. Includes all the features of Single User Advanced BASIC above, plus Text Variables (string manipulation) and Matrix Instructions. This compiler provides our BASIC user with capabilities not usually found in a small machine environment. Runs in 8K Core.

FORTRAN. Similar to ANSI Basic FORTRAN. In addition, it provides such features as N-Dimensional subscripted arrays; extended names; dimensioning with common; unrestricted subscripted expressions; free-field format on input; and extended labels. Does not include equivalence or function definition.

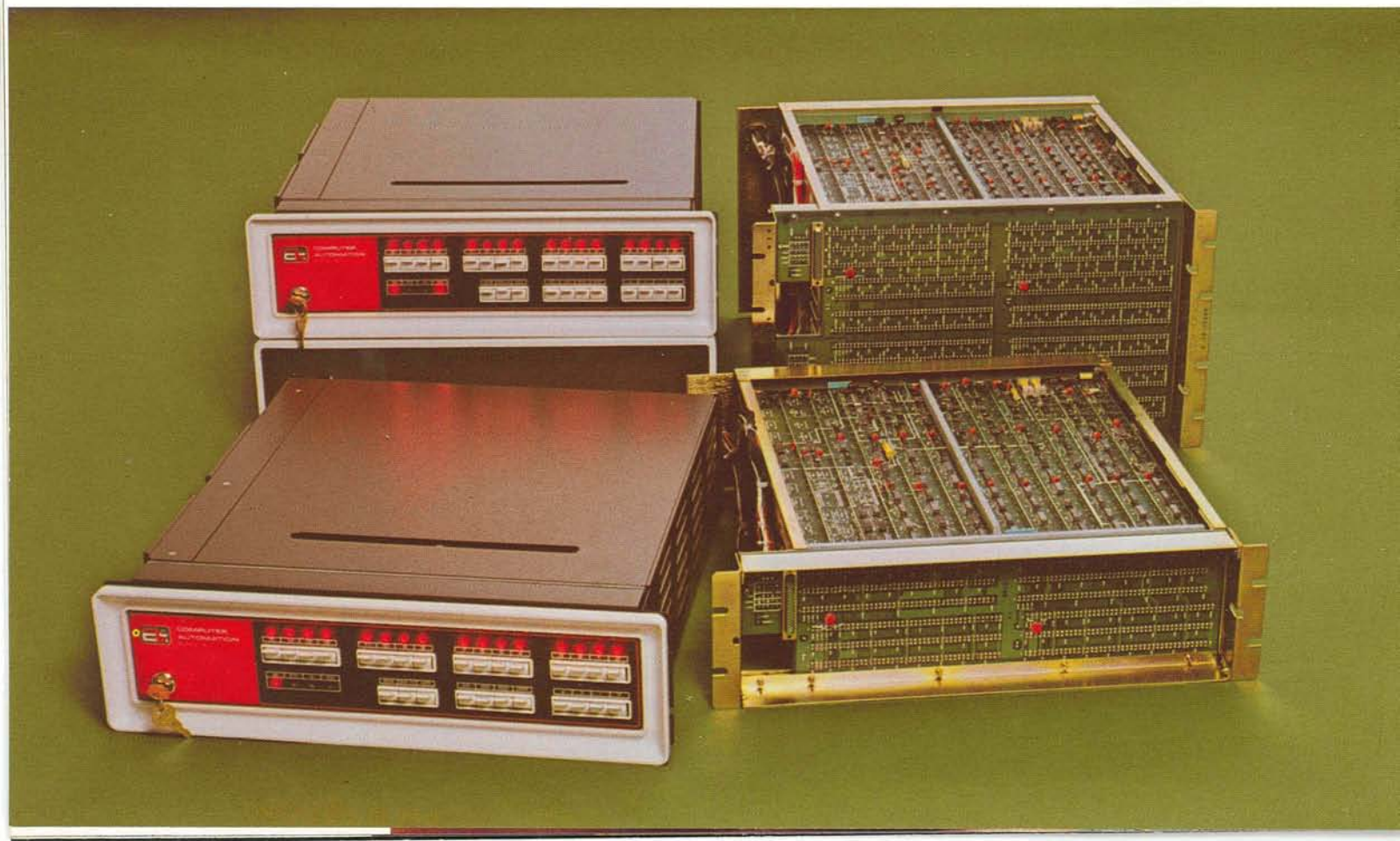
Other Software

BETA Assembler. The Beta Assembler reads a free-form source format, translates it, and generates a relocatable object program. It is a two pass system and is I/O device independent. It provides an operation code definition feature which allows the programmer to rename existing instructions, or to name previously unnamed microcodes. Other significant features are: Symbolic source save (which saves source input code during pass 1 and re-reads it from memory during pass 2 whenever sufficient core storage is available); conditional assembly; and optional error-only listing at assembly time.

OMEGA Conversational Assembler. A conversational, free-form, on-line assembler. In addition to all the features of the BETA assembler, it provides extensive on-line editing and updating capabilities. OMEGA scans entire source programs in core, and at the programmer's option, prints only error flags so that corrections can be made in core before continuing with complete listings and object program tapes.

Source Tape Preparation (STP). STP provides a method of preparing and/or editing symbolic source tapes for input to the BETA assembler. In the preparation mode, the operator enters source lines through the teletype keyboard. Backspace, delete and insert functions allow the operator to correct errors in typing. In the edit mode, the source tape to be corrected is placed in the paper tape reader and editing commands are typed on the teletype keyboard.

In front, ALPHA 16 and NAKED MINI 16; in rear, Jumbo ALPHA 16 and Jumbo NAKED MINI 16.



LAMBDA Object Loader. The LAMBDA loader enables you to load both object program tapes produced by BETA and binary tapes produced by the Binary Dump/Verify Program.

Binary Dump/Verify (BDP/VER). Punches out a specified area of core memory in binary format and optionally verifies the punched tape.

Binary Loader (BLD). Loads binary tapes produced by the Binary Dump Program into core memory. Due to its small size, BLD can load programs which occupy most of memory.

Debug (DBUG). An interactive program which aids the user in debugging his programs. DBUG functions include: fill memory; modify memory; print memory; inspect/change memory; search memory; copy memory; set breakpoint and transfer control.

Teletype Utility Package (TUP). Thirteen object programs which perform the most common teletype input/output functions.

Math 1-Fixed Point Arithmetic Package. Twelve object language programs which perform single and double-precision arithmetic functions.

Math 2-Fixed Point Elementary Functions Package. The twelve most frequently used mathematical functions in fixed point.

Math 3-Floating Point Arithmetic Package. Floating point add, subtract, multiply, divide, compare and fixed-to-floating point and floating-to-fixed point conversion routines.

Math 4-Floating Point Elementary Functions Package. The twelve most frequently used mathematical functions in floating point.

Diagnostics. The Quality Control Diagnostics provide a complete check of the instruction repertoire, memory and certain processor mounted options. Individual diagnostics are provided for each peripheral.

Training

Computer Automation maintains a regular training program in both programming and maintenance.

Two programming courses are offered: one for the beginner who has no computer programming experience at all; and an advanced course for those who have completed the first course or have prior programming experience. Real time programming is stressed. Each course is 40 hours in length, and includes extensive "hands on" laboratory experience.

The maintenance course provides 40 hours of lecture and lab in basic theory of operation and maintenance, and emphasizes the use of computer diagnostic programs. Special courses can be provided as required.

Field service

Computer Automation provides a variety of service arrangements and maintenance alternatives, thus enabling the user to tailor a service program to his particular needs.

On-site maintenance for our equipment is provided by Control Data Corporation's field service organization under a world-wide third party maintenance agreement. CDC can provide 24-hour emergency maintenance service on a per-call basis, or a service contract can be purchased which includes monthly scheduled preventive maintenance plus emergency service coverage.

An alternative is for the user to stock his own spares, which can be purchased at modest cost — typically for less than the cost of a one-year service contract.

Maintenance training emphasizes "hands-on" laboratory experience.

List of instructions

Memory reference

		Cycles
Arithmetic		
ADD	Add to A Register	2
ADDB	Add Byte to A	2
SUB	Subtract from A Register	2
SUBB	Subtract Byte from A	2
MPS	Multiply signed	1¼+½k
DVS	Divide signed	1¼+½k
Logic		
AND	AND to A	2
ANDB	AND Byte with A	2
IOR	Inclusive OR to A	2
IORB	Inclusive OR Byte with A	2
XOR	Exclusive OR to A	2
XORB	Exclusive OR Byte with A	2
Data Transfer		
LDA	Load A	2
LDAB	Load A with Byte	2
LDX	Load X	2
LDXB	Load X with Byte	2
STA	Store A	2
STAB	Store Byte from A	2
STX	Store X	2
STXB	Store Byte from X	2
EMA	Exchange A and Memory	2
EMAB	Exchange A and Memory (Byte)	2
Program Transfer		
JMP	Unconditional Jump	1
JST	Jump and Store P Counter	2
IMS	Increment Memory, Skip on Zero	2
SCN	Scan Memory	2
CMS	Compare A with Memory, skip (high, low, equal test)	2
CMSB	Compare A with Memory Byte, skip (high, low, equal)	2

Conditional jump

Arithmetic		
JAG	Jump if A Greater Than Zero	1
JAP	Jump if A Positive	1
JAZ	Jump if A Zero	1
JAN	Jump if A Not Zero	1
JAL	Jump if A less than or equal to Zero	1
JAM	Jump if A Minus	1
JXZ	Jump if X Zero	1
JXN	Jump if X not Zero	1
Control		
JSS	Jump if Sense Switch Set	1
JSR	Jump if Sense Switch Reset	1
JOS	Jump if OV Set	1
JOR	Jump if OV Reset	1
JOC	Jump on Condition Specified	1

Byte immediate

		Cycles
AXI	Add to X Register Immediate	1
SXI	Subtract from X Register Immediate	1
CAI	Compare to A Immediate, skip if not equal	1
CXI	Compare to X Immediate, skip if not equal	1
LAP	Load A Positive Immediate	1
LXP	Load X Positive Immediate	1
LAM	Load A Minus Immediate	1
LXM	Load X Minus Immediate	1

Register change

Accumulator		
ZAR	Zero A Register	1
ARP	Set A Register to Positive 1	1
ARM	Set A Register to Minus 1	1
CAR	Complement (1's) A Register	1
NAR	Negate A Register	1
IAR	Increment A Register	1
DAR	Decrement A Register	1
Index		
ZXR	Zero X Register	1
XRP	Set X Register to Positive 1	1
XRM	Set X Register to Minus 1	1
CXR	Complement (1's) X Register	1
NXR	Negate X Register	1
IXR	Increment X Register	1
DXR	Decrement X Register	1
Overflow		
SOV	Set Overflow	1
ROV	Reset Overflow	1
COV	Complement Overflow	1
Multi-Register		
ZAX	Zero A and X Register	1
AXP	Set A and X Registers to Positive 1	1
AXM	Set A and X Registers to Minus 1	1
TAX	Transfer A to X	1
TXA	Transfer X to A	1
ANA	AND of A and X to A	1
ANX	AND of A and X to X	1
NRA	NOR of A and X to A	1
NRX	NOR of A and X to X	1
CAX	1's Complement (A) and put in X	1
CXA	1's Complement (X) and put in A	1
NAX	Negate (A) and put in X	1
NXA	Negate (X) and put in A	1
IAX	Increment (A) and put in X	1
IXA	Increment (X) and put in A	1
DAX	Decrement (A) and put in X	1
DXA	Decrement (X) and put in A	1

Shift class

		Cycles
Arithmetic		
NOR	Normalize X	1+¼k
ARA	Arithmetic Right A	1+¼k
ARX	Arithmetic Right X	1+¼k
ALA	Arithmetic Left A	1+¼k
ALX	Arithmetic Left X	1+¼k
Logical		
LRA	Logical Right A	1+¼k
LRX	Logical Right X	1+¼k
LLA	Logical Left A	1+¼k
LLX	Logical Left X	1+¼k
RRA	Rotate Right A with OV	1+¼k
RRX	Rotate Right X with OV	1+¼k
RLA	Rotate Left A with OV	1+¼k
RLX	Rotate Left X with OV	1+¼k
Double		
LRL	Long Rotate Left with OV	1¼+½k
LRR	Long Rotate Right with OV	1¼+½k
LLL	Long Logical Left	1¼+½k
LLR	Long Logical Right	1¼+½k
Control		
SAO	Sign of A to OV	1
SXO	Sign of X to OV	1
LAO	Least significant bit of A to OV	1
LXO	Least significant bit of X to OV	1

Control

Processor		
NOP	No operation	1
HLT	Halt	1
SBM	Set Byte Operand Mode	1
SWM	Set Word Operand Mode	1
TRP	TRAP	1¼
RAM	Set Random Access Mode	1¼
ROM	Set Read Only Mode	1¼
SIN	Status Inhibit	1¼
SIA	Status Input to A	1¼
SIX	Status Input to X	1¼
SOA	Status Output From A	1¼
SOX	Status Output from X	1¼
Interrupts		
EIN	Enable Interrupts	1
DIN	Disable Interrupts	1
CIE	Console Interrupt Enable	1¼
CID	Console Interrupt Disable	1¼
PFE	Power Fail Interrupt Enable	1¼
PFD	Power Fail Interrupt Disable	1¼
MPE	Memory Protect Enable	1¼
MPD	Memory Protect Disable	1¼

Input/Output

		Cycles
Control		
SEL	Select	1¼
SEA	Select and Present A	1¼
SEX	Select and Present X	1¼
SEN	Sense and Skip on Response	1¼
SSN	Sense and Skip on no Response	1¼
ISA	Input Data Switches to A	1¼
ISX	Input Data Switches to X	1¼
Block		
BIN	Input Block to Memory	1¼
BOT	Output Block from Memory	1¼
Automatic		
AIN	Automatic Input to Memory — Word	1¼
AOT	Automatic Output from Memory — Word	1¼
AIB	Automatic Input to Memory — Byte	1¼
AOB	Automatic Output from Memory — Byte	1¼
Conditional		
RDA	Read Word to A	1¼
RDAM	Read Byte to A Masked	1¼
RDX	Read Word to X	1¼
RDXM	Read Word to X Masked	1¼
RBA	Read Byte to A	1¼
RBAM	Read Byte to A Masked	1¼
RBX	Read Byte to X	1¼
RBXM	Read Byte to X Masked	1¼
WRA	Write A	1¼
WRX	Write X	1¼
WRZ	Write Zero's	1¼
Unconditional		
INA	Input Word to A	1¼
INAM	Input Word to A Masked	1¼
INX	Input Word to X	1¼
INXM	Input Word to X Masked	1¼
IBA	Input Byte to A	1¼
IBAM	Input Byte to A Masked	1¼
IBX	Input Byte to X	1¼
IBXM	Input Byte to X Masked	1¼
OTA	Output A	1¼
OTX	Output X	1¼
OTZ	Output Zero's	1¼

ALPHA 16 AND NAKED MINI 16 Specifications

Word Size	16 bits
Memory Size	2K to 32K words (4K std)
Instruction Set	152 plus microcodes
Memory Speed	1.6μsec full cycle
Add/Subtract	3.2μsec
Hardware Multiply (std)	13.2μsec
Hardware Divide (Std)	16.0μsec
DMA (optional)	714,000 words/sec
Block I/O (Std)	416,666 words/sec
Programmed I/O	119,000 words/sec
Automatic I/O on interrupt	100,000 words/sec (via std DMC)
Memory Addressing	Both word and byte
Priority Interrupt	3 standard up to 256
Memory Parity	Optional
Memory Protect	Optional
Physical size:	Mainframe — 5¼" x 19" x 20" Power Supply — 3½" x 19" x 15"

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