6400/6600

CONTROL DATA® 6400/6600...COMPUTING SYSTEMS' CONFIGURATOR

This configurator substantiates Control Data's claim of supplying the world's most powerful computer systems. It merits close scrutiny, because it very quickly charts the combination of speed, versatility, size and ease of use made possible by concurrent operating characteristics available in no other system on the market today.

Through their concurrency, 6400/6600 Systems truly erase data processing limitations that system designers, programmers, and users have formerly had to face. Instead of posing problems, they invite anyone to extend his imagination to keep up with a fresh, intellectually-appealing approach to computing . . . any kind, even though the 6400/6600 Systems are by design especially well equipped to cope with large scientific/mathematical types of problems.

The computer, which at first glance may seem complex, is in reality an ingeniously simple, logical combination of 12 data channels, 10 peripheral/control processors, a large central memory and an ultra high-speed processor. Their unique computing value becomes evident when each is explained according to its working relationship with other elements of the system.

TWELVE DATA CHANNELS

Each data channel is independent and bi-directional, with built-in traffic controls to direct communication in a fast, orderly fashion, between external devices (tape transports, card readers, displays, etc.) and peripheral/control processors. A wide number and variety of external devices may be used, since more than one may be connected to each channel, which is capable of communicating with any peripheral/control processor. Although only one device may be using a channel at a time, all twelve channels may be operating simultaneously, and at this point, evidence of the concurrency that gives a 6000 Series a competitive edge begins to emerge.

Data is accepted in the form of 12-bit words, and transferred to peripheral processors in blocks of words. These blocks may range in size from one word to "n" words.

SPEED: One 12-bit word every 1000 nanoseconds.

TEN PERIPHERAL/CONTROL PROCESSORS

Each is a stored-program computer with its own 4K, 12-bit-word, random-access memory. Each operates simultaneously with and independently of the other processors, so that 10 programs may be operating in the processors at the same time. The programs handle overall system control and all input/output processing. By assuming these tasks, they free the central processor and central memory from time-consuming, space-consuming menial labor and housekeeping chores.

Programs for the ten processors are written in a conventional batch-processing manner, but are executed on a time-shared basis in an instruction control slot and register barrel common to all the processors.

Data is then assembled from 12-bit words into 60-bit words and sent to central memory. On the way from central memory to peripheral/control processors, the 60-bit words are disassembled into 12-bit words at this point.

SPEED: Each peripheral processor program is acted upon once every 1000 nanoseconds.

CENTRAL MEMORY

The central memory is made up of banks of 4K 60-bit words. It may be 8, 16 or 32 banks with a total of 32, 65 or 131K words.

All banks are logically independent, and consecutive addresses go to different banks, so that several banks may be in operation simultaneously . . . another example of concurrency. All banks may be referenced by the peripheral/control processors as well at the central processor, with two devices directing the flow of information:

1) A stunt box acts as a clearing house for all addresses, issuing and reissuing them under priority control until they can be assigned to memory bank. 2) A data distributor handles all data words moving to and from central memory, and provides temporary storage for those words whose addresses are not immediately accepted because of memory-bank conflicts.

Full memory protection is provided by special instructions which define upper and lower limits of any central memory program.

SPEED: Central memory major cycle is 1000 nanoseconds.
Central memory minor cycle is 100 nanoseconds.

TABLE B – EXTENDED CORE STORAGE			
MODEL NO.	CAP. CHAR.	AVG. ACCESS TIME	TRANSFER RATE (60-BIT WORDS)
6633	131K	3 μSEC.	2.5 M/SEC.
6634	262K	"	5 M/SEC.
6635	524K	"	10 M/SEC.
6636	1048K	"	10 M/SEC.

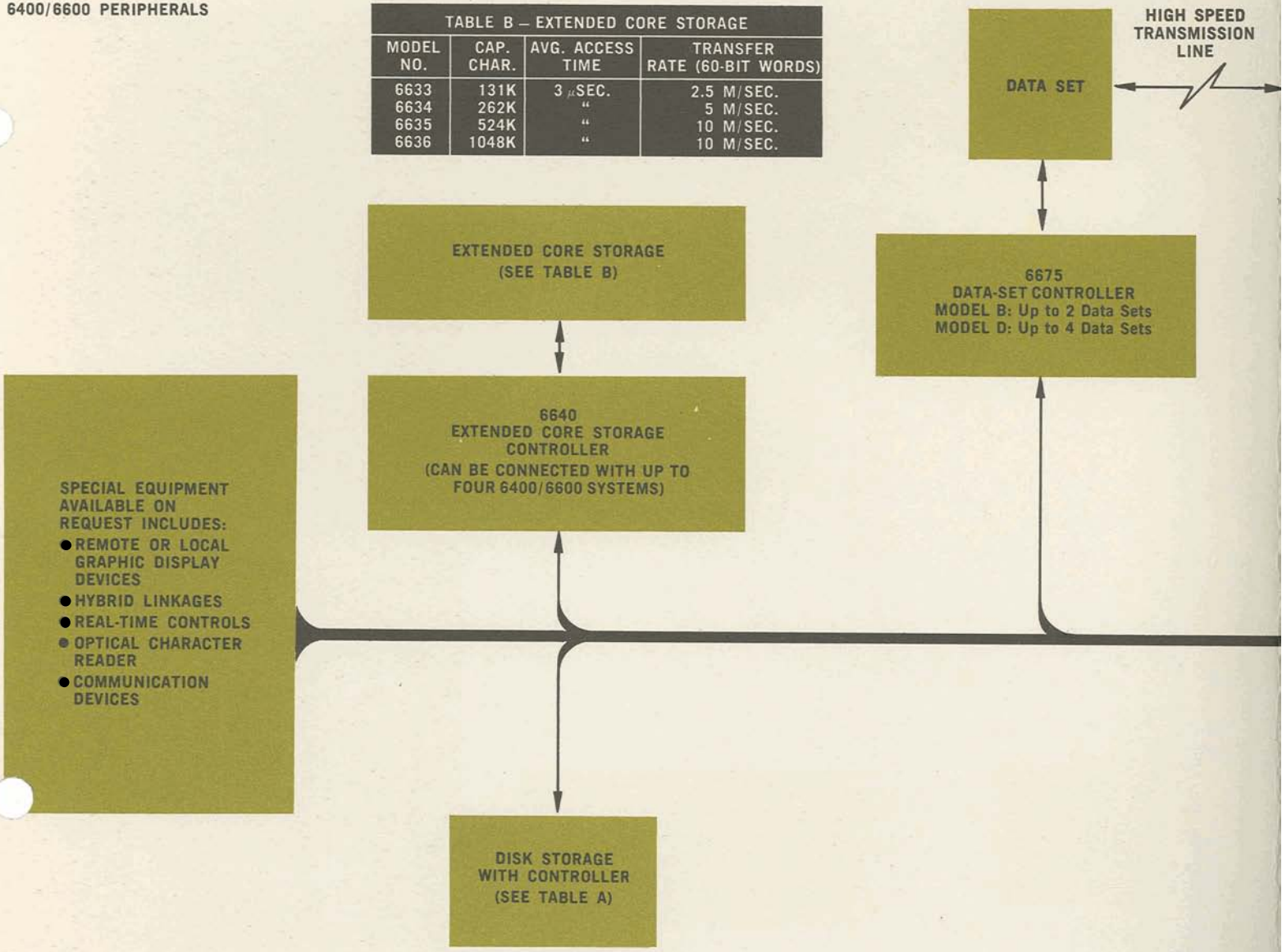
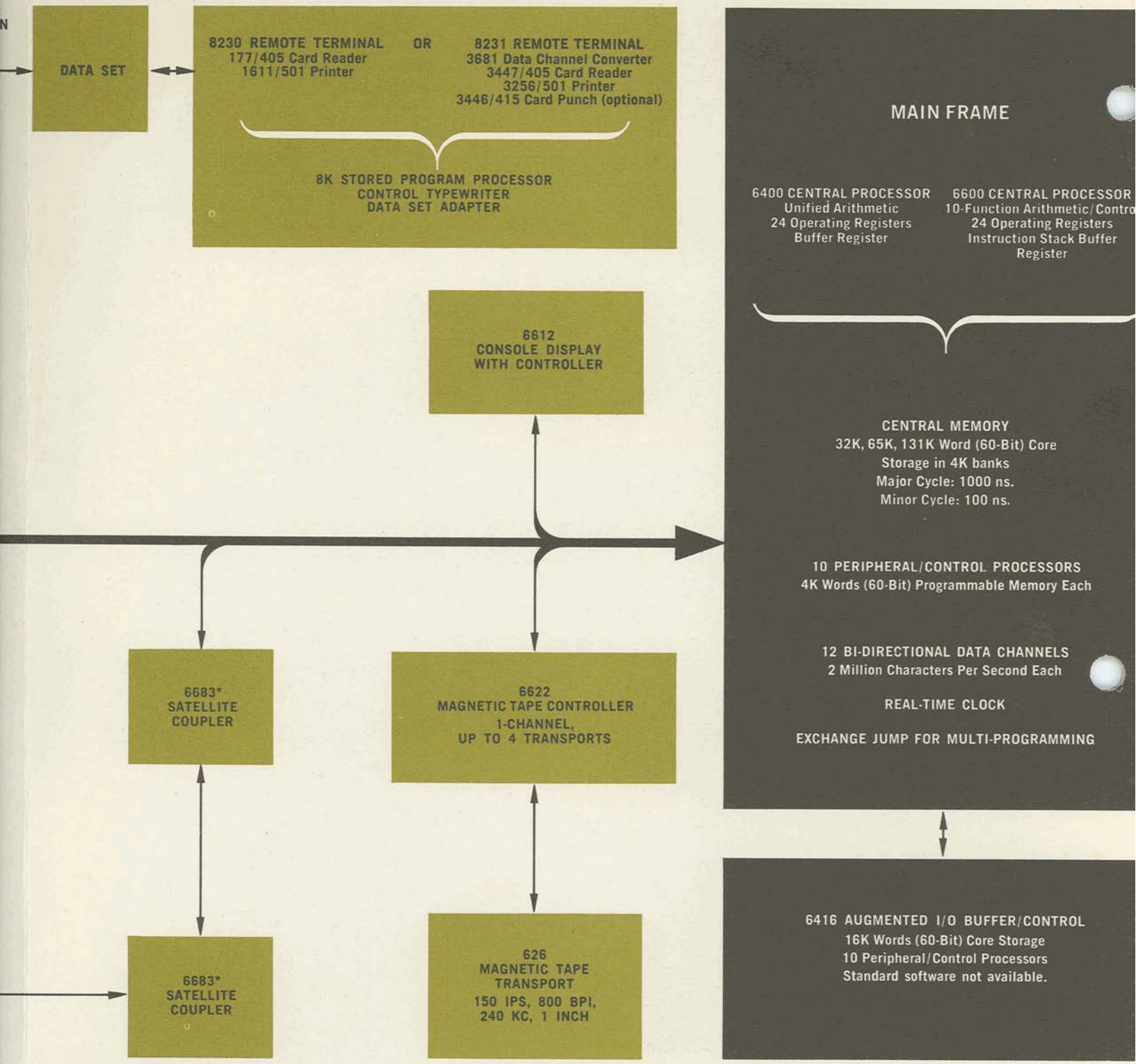


TABLE A – DISK STORAGE				
MODEL NO.	NO. OF CHANNELS	CHARACTER CAPACITY	AVG. ACCESS TIME	TRANSFER RATE (CHAR.)
6603	1	74M	270 Ms	1.25 M/SEC.
6638	1*	168M	100 Ms	1.68 M/SEC.

*2 channel access with option 10037, standard software not available.

ANOTHER 6400/6600 SYSTEM



*Standard software not available.

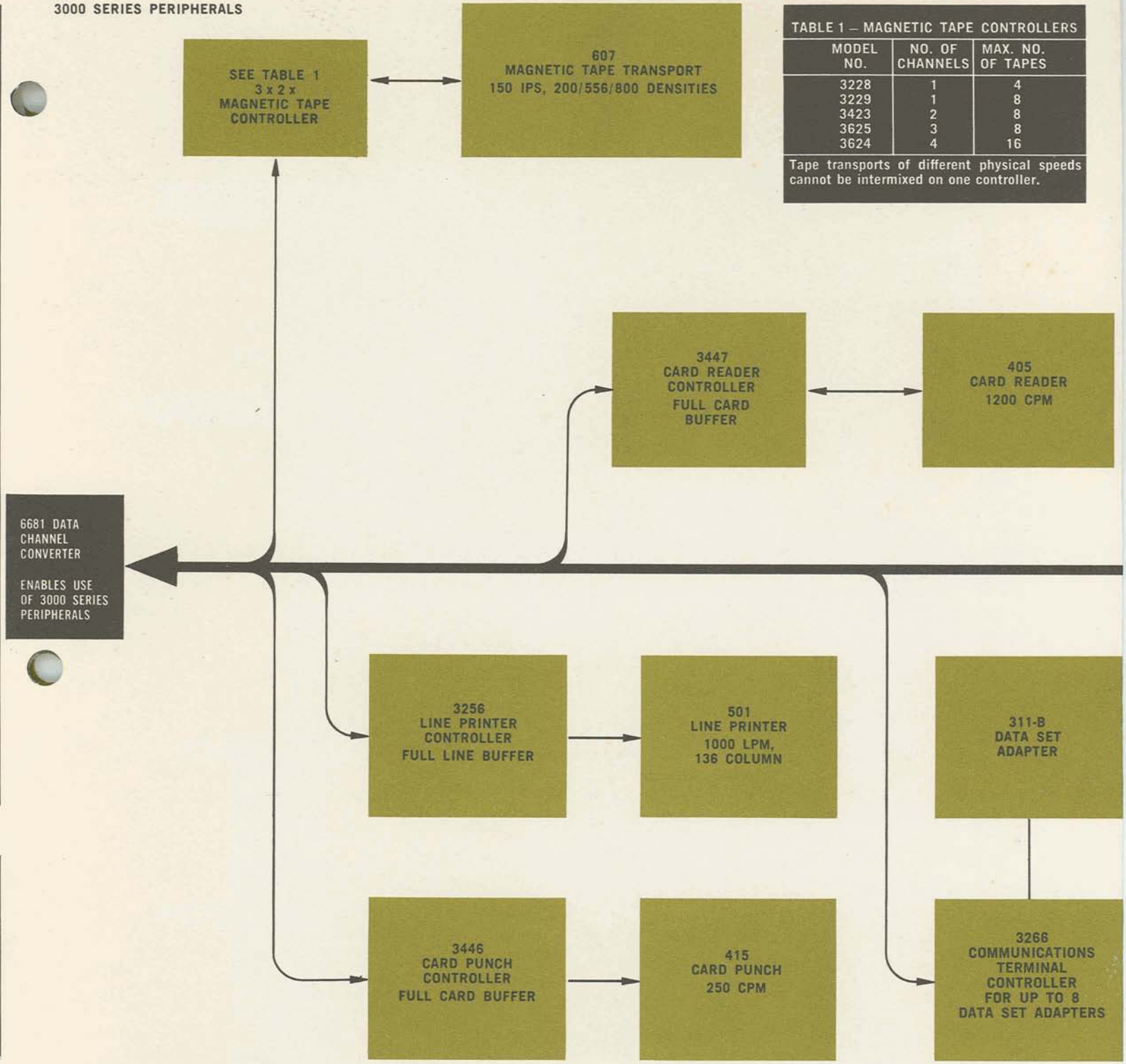


TABLE 1 – MAGNETIC TAPE CONTROLLERS

MODEL NO.	NO. OF CHANNELS	MAX. NO. OF TAPES
3228	1	4
3229	1	8
3423	2	8
3625	3	8
3624	4	16

Tape transports of different physical speeds cannot be intermixed on one controller.

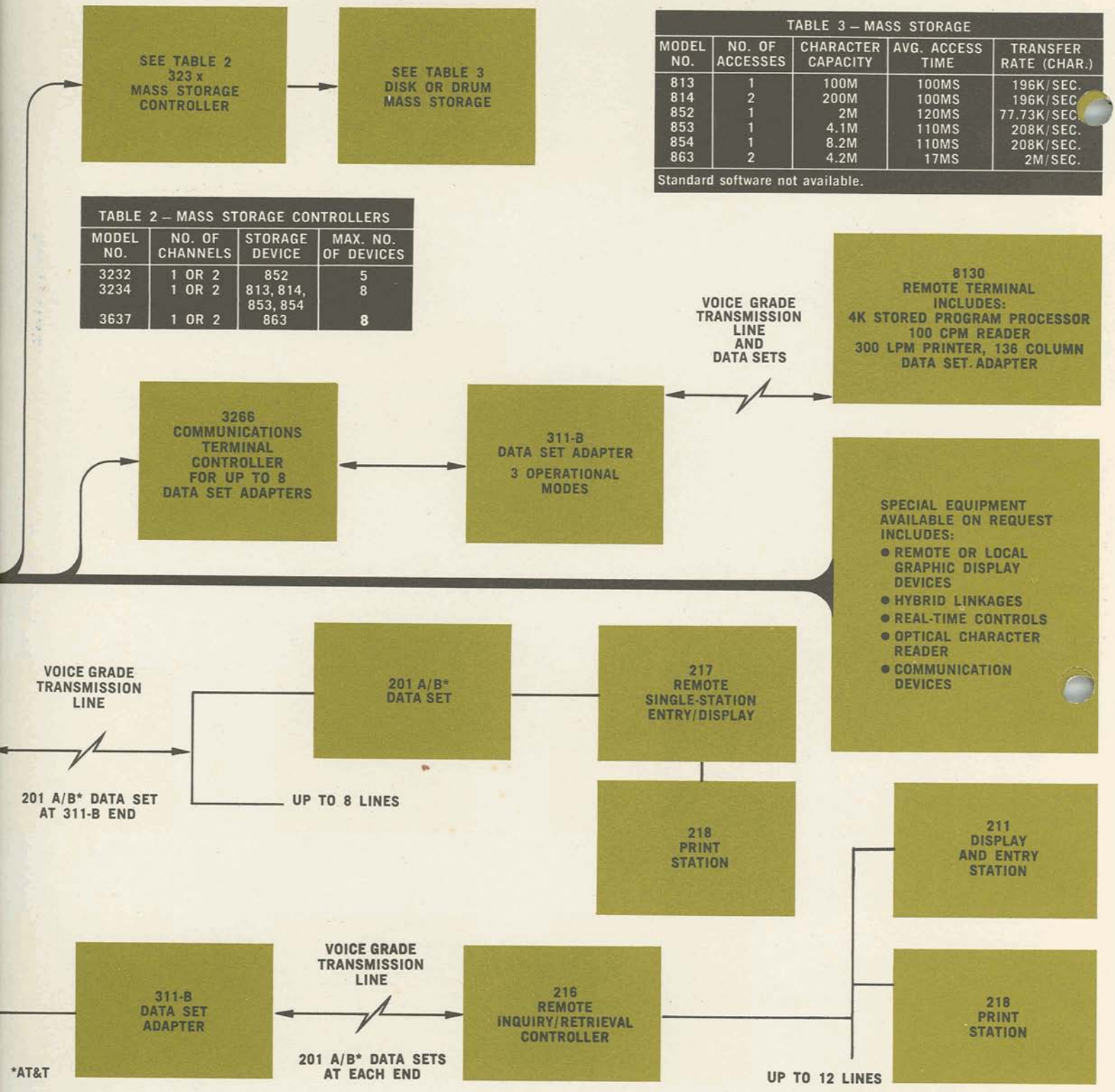


TABLE 3 – MASS STORAGE

MODEL NO.	NO. OF ACCESSES	CHARACTER CAPACITY	AVG. ACCESS TIME	TRANSFER RATE (CHAR.)
813	1	100M	100MS	196K/SEC.
814	2	200M	100MS	196K/SEC.
852	1	2M	120MS	77.73K/SEC.
853	1	4.1M	110MS	208K/SEC.
854	1	8.2M	110MS	208K/SEC.
863	2	4.2M	17MS	2M/SEC.

Standard software not available.

TABLE 2 – MASS STORAGE CONTROLLERS

MODEL NO.	NO. OF CHANNELS	STORAGE DEVICE	MAX. NO. OF DEVICES
3232	1 OR 2	852	5
3234	1 OR 2	813, 814, 853, 854	8
3637	1 OR 2	863	8

CENTRAL PROCESSOR

Communicates only with central memory, except on an exchange jump operation, which starts or interrupts the central processor from a peripheral processor and monitors a central program address from a peripheral processor.

All communications between the central processor and central memory are made through a set of 24 operating registers. The registers are broken down into three groups: Eight 18-bit address registers, eight 18-bit index registers and eight 60-bit operand registers.

This arrangement benefits overall operation by minimizing central memory references.

From this point on, the central processor operations differ for the 6400 and 6600; therefore, each will be explained separately.

The 6400 utilizes a unified arithmetic section that executes instructions sequentially. The flow of instructions to and from the operating registers is monitored by a traditional buffer register.

The 6600, on the other hand, utilizes a 10-function arithmetic section, and an instruction stack instead of the buffer register. Both devices add their own kind of concurrency, greatly increasing speed and efficiency. All 10 functional units can operate simultaneously with one or more of the other units. The instruction stack, eight 60-bit high-speed registers, is designed so that a great many "short loops" can be held in the stack until all iterations are complete. While in the stack, they do not prevent the concurrent entering and execution of other instructions. They are simply moved up in the stack while being executed, making room for new instructions coming in. A scoreboard keeps track of all instructions in the stack, removing those which are completed.

An additional example of concurrency results from the combination of the sets of ten functional units and three types of operating registers. The instruction format allows each of the 10 functional units to obtain two 60-bit operands from the operating registers, produce a 60-bit result and return it to an operating register using only one instruction.

TRANSITION TO SOFTWARE

By now, it should be obvious that the 6400/6600 Systems offer an open invitation to explore not only new solutions to old problems, but entirely new approaches to data processing. Overall system concepts are extended far beyond previous limitations. Maximum concurrency opens the door to many unusual techniques. Among them:

- Optimization of multi-processing and multi-programming.
- Time-sharing of a great many and varied I/O devices.
- Top level swiftness and efficiency in handling lengthy, complex scientific/mathematical problems.

SOFTWARE

The software package for the 6400/6600 Systems is designed to complement and to maximize the operating characteristics of the hardware. Organized in product sets, the package offers an overall operating system and subordinate programs. The approach is traditional. Languages used are those which are familiar to the programmer. Results are unique.

The operating system is designed to reside in peripheral processor memory, requiring little central memory space or time while in operation, performing housekeeping chores and monitoring the flow of data into and out of the system.

Specifically designed for use with the operating system are:

- Assemblers with symbolic instruction, system macros, programmer-defined macros and pseudo-commands.
- Compilers featuring a new, more powerful, Fortran with ASA compatibility and an automatic, built-in capability for fully utilizing the concurrency of the central processor. Other compilers include COBOL and ALGOL.
- Special programs are available to help with the management of information. These include SORT/MERGE for automatic file maintenance, plus PERT-TIME and a special File Manager.
- SIMSCRIPT for simulation programming.
- APT for numerically-controlled machine tools.
- LP for linear programming.
- KWIC for speedy retrieval of information from data files.
- Special subroutines for performing statistical functions, and matrix algebra, and for the use of extended core storage.

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CONTROL DATA
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